REMARKS

The Examiner is thanked for the thorough examination of the present application, and the indication that claim 23 would be allowable if rewritten in independent form. This response is in reply to the Office Action of Jan. 10, 2006.

Response To Claim Rejections Under 35 U.S.C. §102

The 102(b) rejections of claims 24, and 27-28 are rendered moot by the cancellation of claims24-28.

Response To Claim Rejections Under 35 U.S.C. §103

Claims 19-22 and 29-32 stand rejected under 35 U.S.C. §103 as allegedly being unpatentable over *Liang* (U.S. Patent No. 5,877,523) in view of *Sekariapuram* (U.S. Patent No. 6,091,102). Applicant respectfully traverses this rejection for at least the reasons set forth below.

Claim 19-22

There is no suggestion in the cited prior art about the desirability of the claimed invention.

"In determining the propriety of the Patent Office case for obviousness in the first instance, it is necessary to ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the reference before him to make the proposed substitution, combination, or other modification." *In re Linter*, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972). "There must be some reason, suggestion, or motivation

found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination." *In re Oetiker*, 977 F.2d 1443, 1447, 24 USPQ 2d 1443 (Fed. Cir. 1992).

Independent claim 19, as original presented, recites the following:

> 19. A multi-level, multi-bit stacked gate flash memory cell structure comprising:
> ***floating gate spacers having convex walls facing each other, and vertical outside walls;***
> ***a conformal dielectric layer covering said convex walls of said floating gate spacers;***
> ***a control gate therebetween said convex walls of said floating gate spacers with intervening said conformal dielectric layer***, and
> insulative spacers formed on said vertical outside walls of said floating gates.

(*Emphasis added*). Claim 19 patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above.

The Office Action indicates that it is *Sekariapuram* but not *Liang* teach the features highlighted above in claim 19, and that the motivation for the modification is taught by *Sekariapuram* in Col. 1, lines 29-38 to improve operating characteristics. Applicant disagrees, as *Sekariapuram* fails to propose what in *Liang* should be substituted, combined, or modified. In this regard, *Sekariapuram* states (in Col. 1, lines 29-38):

> As integrated circuit and semiconductor processing technologies continue to advance, there is a need for greater densities and functionality in integrated circuits. These are often determined in a large part by the size and structure of the memory cells. Further, it is desirable that the memory cells have improved operating characteristics, such as lower power consumption, nonvolatility, reprogrammability, greater device longevity, improved data retention, better transient performance, superior voltage and current attributes, and improvements in other similar attributes.

In view of the above teaching, it is the whole memory cell (not merely parts of the memory cell) disclosed by *Sekariapuram* that obtain the operating characteristic improvement. Nowhere does *Sekariapuram* teach to a person skilled in the art that only the features

emphasized above contribute to the operating characteristic improvement. Since the memory cell of *Sekariapuram* surpasses that of *Liang* in every aspect, the memory cell of *Sekariapuram* as a whole should replace that of *Liang*. The motivation to partially modify a memory cell as indicated by the Office Action cannot be expressly or inherently found in *Sekariapuram*. Therefore, the reference teachings of *Liang* and *Sekariapuram* are insufficient for one of ordinary skill in the art having the references before him to make the proposed substitution, combination, or other modification mentioned by the Office Action. For at least this reason, the rejection of claim 19 should be withdrawn.

Teachings of *Sekariapuram*, even if combined with *Liang*, conflicts with the formation of the insulative spacers in *Liang*.

> If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)

Sekariapuram teaches, in all figures, memory cells in trenches, such that the channel of a memory cell is located in the sidewall of a trench. In other words, *Sekariapuram* requires a conductor on the vertical outside walls of the floating gates in a memory cell. The formation of insulative spacers on the vertical outside walls of the floating gates would be viewed as prohibited by persons skilled in the art, since it will stop the formation of a channel. *Liang*, on the other hand, teaches the formation of a channel under the floating gates, such that the insulative spacers can be formed on the vertical outside walls of the floating gates. Since the teachings of *Sekariapuram* conflict with the teachings of *Liang* to assemble the claimed invention of claim 19, there is no proper suggestion or motivation to make the proposed modification required by the Office Action.

For at least the reasons set forth above, claim 19 patently defines over the cited art. For at least the same reasons, dependent claims 20-22 also define over the cited art. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Claim 29-32

Independent claim 29, as previously presented, recites:

> 29. A multi-level, multi-bit stacked gate flash memory cell structure, comprising:
> two floating gates on an insulating layer on a substrate, having opposite sidewalls facing each other;
> a conformal dielectric layer covering opposite sidewalls of the two floating gates;
> a control gate therebetween the opposite sidewalls of the two floating gates with intervening the conformal dielectric layer;
> two insulative spacers covering outside walls of the two floating gates; and
> ***further comprising a first, second and third doped regions in the substrate as source/drain regions, wherein the first doped region is disposed between the two opposite sidewalls of the two floating gates, and the second and third doped regions are disposed outside of the outside walls of the two floating gates respectively.***

(*Emphasis added*). Claim 29 patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above.

Similar to the discussion set forth for the patentability of claim 19, there is no proper motivation why the features highlighted above in claim 29 and taught in *Sekariapuram* should be added into the memory cell of *Liang*. The motivation to partially modify a memory cell as required by the Office Action cannot be found in *Sekariapuram*. Furthermore, the teachings of *Sekariapuram* conflict with the teachings of *Liang* regarding to the formation of insulative spacers, such that there is no suggestion or motivation to make the proposed modification as

indicated by the Office Action. For at least this reason, claim 29 patently defines over the prior art of record.

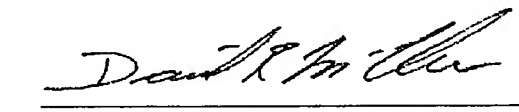
Because independent claim 29 is allowable, dependent claims 30-32 are allowable as a matter of law. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: 

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